IN THE UNITED STATES PATENT AND TRADEMARK

Assistant Commissioner for Patents
Washington, D.C. 20231

Attorney's Docket No.: 15962-0012

FILING TRANSMITTAL

Transmitted herewith for filing is the Patent Application of: Chen

For: **"Methods and Circuits for Power Management in a Transceiver"**

ENCLOSURES

☒   12 page application including specification, claims and abstract;
☒   2 sheets (Figs. -) of ☒ informal/☐ formal drawings;
☒   A Declaration, Power of Attorney & Petition (☒ signed/☐ unsigned);
☐   A postcard for return to us as proof of receipt of the referenced documents.
And
☐   An Assignment of the invention with an assignment cover sheet;
☒   Verified Statement Claiming Small Entity Status (37 CFR 1.9(f) and 1.27(b));
☐   IDS (form PTO-1449) and copies of references;
☐   An Associate Power of Attorney;
☐   A certified copy of the priority document (Under 35 USC 119);
☐   A Power of Attorney by Assignee;
☐   Other.
TYPE OF FILING
☒   This application claims the benefit of an earlier filed U.S. Patent Application (35 USC 120).
☒   This application claims the benefit of the priority date of an earlier filed patent application (35 USC 119).
☐   This is an application filed pursuant to 37 CFR 1.53, permitting receipt of a filing date upon filing of specification, claims and drawings, if required, with applicant being given a period of one month from the date of notice to file the fee and oath or declaration.
☐   In the event any parts of this application are missing, please treat this as a filing under 37 CFR 1.53 as defined just above.

CERTIFICATE OF MAILING (37 CFR 1.10(a))
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Date: 10/8/99
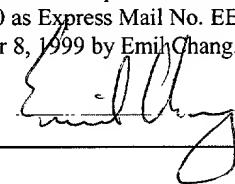
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FEE CALCULATION

The filing fee has been calculated as shown below:

|			SMALL ENTITY	OR	OTHER THAN A SMALL ENTITY	
BASIC FEE Design Patent			$155	$	$310	$
BASIC FEE Utility Patent			$380	$ 380	$760	$
EXTRA FEES			RATE	FEE	RATE	FEE
Total claims	minus	=	x9 =	$	x18 =	$
Independent Claims	minus	=	x39 =	$	x78 =	$
☐ Multiple Dep. Claim			+130 =	$	+260 =	$
☐ Assignment			+40 =	$	+40 =	$
☐ Rule 53 Surcharge			+65 =	$	+130 =	$
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☑ The filing fee and surcharge under 37 CFR 1.16, patent application processing fees under 37 CFR 1.17 and patent issue fees under 37 CFR 1.18 are intended to be paid by our firm as they arise. As no abandonment is intended by any inadvertent nonpayment of fees, the Commissioner is hereby authorized to charge payment of such fees as from time to time come due, <u>if not paid prior to due date</u> to our Deposit Account No. 02-3964.

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Dated: 10/8/99

Respectfully submitted,
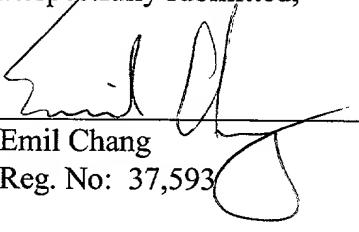
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Attorney's File No: 15962-0012
Applicant or Patentee: Chen
Serial: _____ Filed: October 8, 1999

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) AND 1.27(c) - <u>SMALL BUSINESS CONCERN</u>

I am:

    ☐   the owner of the small business concern identified below;

    ☒   an official of the small business concern empowered to act on behalf of the concern identified below;

Name of Concern: Altima Communications, Inc.

Address of Concern: 2055 Gateway Place, #700, San Jose, CA, 95110

I hereby declare that the above-identified small business concern qualifies as a small business concern as defined in 13 CFR 121.318, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees under section 41(a) and (b) of Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full time, part-time, or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention entitled: "Methods and Circuits for Power Management in a Transceiver" by Xi Chen described in:

        ☒   the specification filed herein
        ☐   Application Serial No: _____
                filed: _____
        ☐   Patent No.: _____
                issued: _____

If the rights held by the above-identified small business concern are not exclusive, each individual, concern or organization having rights to the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who could not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

*NOTE: Separate Verified Statements are required from each named person, concern, or organization having rights to the invention averring to their status as small entities (37 CFR 1.27)

NAME: _____

ADDRESS: _____

      ☐ INDIVIDUAL   ☐ SMALL BUSINESS   ☐ NONPROFIT ORGANIZATION

I acknowledge my duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, earliest of the Issue Fee or any Maintenance Fee due after the date on which status as a small entity is no longer appropriate (37 CFR 1.28(b)).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of

Title 18 of the United States Code, and that such willful, false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this Verified Statement is directed.

Name of Person Signing:	Emil Chang
Title:	General Counsel
Address of Person Signing:	2055 Gateway Place, #700, San Jose, CA, 95110.

Signature:
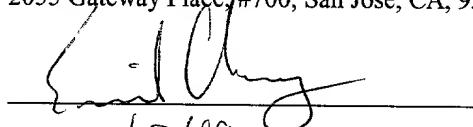
Date: 10/8/99

1   **Specification**

2

3   **METHODS AND CIRCUITS FOR POWER MANAGEMENT**

4   **IN A TRANSCEIVER**

5

6   **PRIORITY CLAIM**

7   This application claims priority to a provisional application entitled "Reset and

8   Power Management" filed on October 8, 1998, having an application number _____.

9

10   **BACKGROUND OF THE INVENTION**

11

12   **Field of the Invention**

13   The present invention generally relates to methods and circuits for power

14   management, and in particular, to methods and circuits for power management in network

15   transceivers.

16

17   **Description of the Prior Art**

18   In a network, there are generally one or more servers connected to a number of client

19   machines via one or more hubs (or repeaters) and or switches. In each one of these devices,

20   there may be one or more transceivers. Each transceiver, if connected to another transceiver,

21   communicates with that transceiver. For example, generally speaking, a server machine has

22   a network card, and there is a transceiver on the network card. If the server is connected to a

1   repeater, it would be connected to the repeater at one of its ports and there would be a

2   transceiver at this port (and each port of the repeater) communicating with the server in

3   accordance with established protocols.

4   The manner in which the transceivers communicate with each other in an Ethernet

5   environment is dictated by IEEE 802.3u. In the specification, it is specifically provided that

6   for a 10 mb (mega bit per second) transceiver, during idle period (when the transceiver is not

7   connected to another transceiver), the transceiver is required to transmit an idle signal to

8   signal the existence of a live transceiver. In this manner, if another transceiver is connected

9   to this transceiver, the two transceivers will detect the existence of each other and initiate

10   communication protocol and transmit and receive data. Fig. 1a illustrates the industry

11   standard specified normal link pulse ("nlp") for transmission in the 10 mb mode. Note that

12   there is a single pulse 10 every 16 ms. For 10 mb auto negotiation mode, referring to Fig.

13   1b, the industry specification requires that there be pulses separated by 16 ms intervals and

14   each pulse 12 having a duration greater than a predefined duration. For 100 mb transceivers,

15   referring to Fig. 1c, the signal type MLT3 having 3 levels of signaling is used.

16   While the industry specifications provide the idle signal type for each mode of

17   operation, for 10/100 mb transceivers, the MLT3 type idle signal is specified. The

18   disadvantage with this specification is that the MLT3 signal consumers a high amount of

19   energy even when there is no activity. It increases power consumption and requires higher

20   cooling requirement – all results in higher system cost.

21   There is much advantage that can be had if the power consumption level of the

22   transceiver can be minimized. For example, if a repeater uses transceivers with low power

-2-

1   consumption, the repeater may be designed without the use of a mechanical cooling fan.

2   The lack of a cooling fan translates to lower overall system cost and higher system reliability

3   (there is not a fan to fail). For the 10/100 mb transceivers, there are many opportunities for

4   power savings if the circuits is designed to minimize power use.

5   Therefore, it is desirable to have a transceiver device with low power consumption.

6

7   **SUMMARY OF THE INVENTION**

8   It is therefore an object of the present invention to provide methods and circuits for

9   low-power transceiver devices.

10   It is another object of the present invention to provide methods and circuits for

11   minimizing power consumption during idle period.

12   It is yet another object of the present invention to provide methods for dividing a

13   10/100 mb transceiver into subcircuits in order to minimize power consumption.

14   Briefly, in a presently preferred embodiments of the present invention, a transceiver

15   circuit having 10 mb and 100 mb transmit and receive circuitries using the power saving

16   methods of the present invention is disclosed. The power consumption of the transceiver

17   circuit can be significantly reduced by providing each defined subcircuit with its own power

18   supply and means of activation and deactivation. However, the method for activating and

19   deactivating digital subcircuits and analog subcircuits are different and therefore different

20   types of control signals and methods are provided. Furthermore, there are two general types

21   of power-saving situations. The first type is near total circuit power-down and the second

1   type is partial circuit power-down. The present invention in yet another embodiment

2   discloses a method for minimizing energy usage during idle period.

3   An advantage of the present invention is that it provides methods and circuits for

4   low-power transceiver devices.

5   Another advantage of the present invention is that it provides methods and circuits

6   for minimizing power consumption during idle period.

7   Yet another advantage of the present invention is that it provides methods for

8   dividing a 10/100 mb transceiver into subcircuits in order to minimize power consumption.

9   These and other features and advantages of the present invention will become well

10   understood upon examining the figures and reading the following detailed description of the

11   invention.

12

13   **IN THE DRAWINGS**

14   Fig. 1a illustrates the waveform of normal link pulse.

15   Fig. 1b illustrates the waveform of fast link pulse.

16   Fig. 1c illustrates the waveform of a MLT3 signal.

17   Fig. 2 illustrates a clock management summary table of the preferred embodiment.

18   Fig. 3 illustrates a power management logic control table of the preferred

19   embodiment.

20   **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

21   In a presently preferred embodiments of the present invention, a transceiver circuit

22   having 10 mb and 100 mb transmit and receive circuitries using the power saving methods

1   of the present invention is disclosed. The power consumption of the transceiver circuit can

2   be significantly reduced by providing each defined subcircuit with its own power supply and

3   means of activation and deactivation. However, the method for activating and deactivating

4   digital subcircuits and analog subcircuits are different and therefore different types of control

5   signals and methods are provided. Furthermore, there are two general types of power-saving

6   situations. The first type is near total circuit power-down and the second type is partial

7   circuit power-down.

8   In the first type of power-saving situation, two power-saving modes are provided. In

9   the first power-saving mode, the transceiver circuit is powered-down. This may be achieved

10   by providing a register and setting the proper register value to activate the power-down

11   mode, or providing a signal to a signal line to the transceiver circuit. In this mode, except

12   for allowing management transactions (by writing to a management register) to the

13   transceiver circuit, all power to other areas of the transceiver circuit is powered off, thus

14   achieving maximum power saving.

15   In the second power-saving mode (for near total circuit power-down), by asserting

16   the proper signal or register value, the present invention provides for nearly total power-

17   down when either (1) there is no valid signal on the media or (2) when there is no valid data

18   at the data interface (also known as media independent interface or MII). For the case where

19   there is no valid data on the MII, most of the subcircuits of the transceiver can be powered-

20   down.

21   For the case where there is no valid signal on the media (e.g. the transceiver is not

22   connected to another transceiver), an analog energy-detect circuit is turned on to monitor for

1 the existence of a signal on the media, and the serial management interface (or SMI) is

2 turned on to allow for any management transaction (for managing the transceiver device).

3 The rest of the receive circuits, which include all of the analog and digital circuits in the

4 receive path, are turned off.

5 Furthermore, the transmit circuit of the transceiver of the present invention sends out

6 an idle signal in accordance with the present invention. The link pulses of the preferred

7 embodiment for the 10/100 transceiver is a short duration pulse recurring every predefined

8 period (preferably every 16ms) like the industry specified normal link pulse (nlp) for

9 10baseT transceiver circuits. Although, the industry specification requires the MLT3 signal

10 type to indicate a live connection on the media for 10/100 transceiver circuits. However, the

11 MLT3 signal type consumes more power than otherwise. In the 10/100 transceiver of the

12 present invention, a normal link pulse is used rather than the MLT3 pulse.

13 Upon receiving activity on the media, the transceiver circuit of the present invention

14 immediately changes to a MLT3 type signal and enters into auto-negotiation mode (if

15 activated). In this manner, although contravening industry specification, only minimal

16 energy is used to indicate that the transceiver is alive and available. If the energy-detect

17 circuit detects signal energy on the media, the receive circuit is turned on immediately. If

18 the energy-detect circuit does not detect signal energy on the media after a predefined period,

19 the transceiver circuit is powered down as described above.

20 For partial circuit power-down type of power saving methods, the transceiver of the

21 present invention uses two clock management and power management to manage power

22 consumption. Note that for digital circuits, stopping the clock to a particular circuit block

1   effectively powers the block down, and for analog circuits, power down is achieved by

2   asserting the power-down pin for the corresponding block.

3   Several clock signals are provided with the transceiver of the present invention. A

4   clk_free clock signal provides a free running 25 MHz clock buffered from a crystal circuit; a

5   clk_tx clock signal provides a free running 20/25 MHz transmit clock synthesized by a

6   transmit PLL circuit where the clock frequency is controlled by another signal; and a clk_rx

7   clock signal provides a 20/25 MHz Recovery clock where the frequency of this clock is

8   controlled by another signal and this clock signal locks to clk_tx when no data is presented

9   on the media and it is locked to the data when it is detected.

10   Additionally, several other clock signals are provided to the digital portion of the

11   transceiver of the present invention. A bt_txc_20 signal provides a 20 MHz transmit clock

12   for 10 BaseT circuit; a bt_rxc_20 signal provides a 20 Mhz recovery clock for 10BaseT

13   circuit; a tx_txc signal provides 25 MHz transmit clock for 100 BaseT 100Base FX circuit; a

14   tx_rxc signal provides 25 MHz recovery clock for 100 BaseT 100Base Fx circuit; a mii_txc

15   signal providing a 25/2.5/10/25/20 MHz transmit clock for MII-100/MII-10/MII-10-

16   Serial/SYM-100/SYM-10 interface; a mii_rxc 25/2.5/10/25 MHz recovery clock for MII-

17   100/MII-10/MII-10-Serial/SYM100 interface; a cp_arb clock for auto-negotiation/arbitration

18   circuit. The timers, mii-management, and led circuit of the transceiver of the present

19   invention use the clk_free clock signal directly, which is always on. The mii-management

20   and timers circuits need to have the clock signal even in power down mode in order to

21   control the transceiver.

1   Referring to Fig. 2, a clock management summary table of the preferred embodiment

2   is illustrated. Here, the operation modes are listed in the column titles. It can be seen that

3   during the power-down mode, all of the clock signals are off to save power. In the energy-

4   detect mode, only the mii_txc and cp_arb clock signals are activated to run the

5   corresponding circuits. In the auto-negotiation mode, the mii_txc and cp_arb signals are

6   activated to conduct the auto-negotiate task. During 10 BaseT operation, the clock signals

7   for the 100 BaseT circuits are turned off. Likewise, during 100 BaseTx operation, the clock

8   signals for the 10 BaseT circuits are turned off. For serial 10 BT operation, the clock signals

9   for the 100 BaseT circuits are turned off. For the FX mode, the clock signals for 10 BaseT

10   operation and cp_arb signal are turned off. For test loop back operation, this operation is

11   conducted using 100 BaseT clock signals. For PCS (Physical Coding Sublayer) bypass 10

12   operation, the clock signals for the 100 BaseT circuits are turned off as well as the mii_rxc

13   and cp_arb signals. For PCS bypass 100 operation, the clock signals for the 10 BaseT

14   circuits are turned off as well as the mii_txc and cp_arb signals. As can be seen here, each

15   clock signals corresponds to certain digital circuit blocks in the transceiver of the present

16   invention. By turning off a clock signal, the corresponding circuit block of the transceiver is

17   turned off.

18   For the analog portion of the transceiver of the present invention, a number of clock

19   signals are provided as well. A mr_pd_pll signal controls the power to the transmit-PLL and

20   clock recovery circuit. A mr_pd_equal signal controls the power to the equalizer and slicer.

21   A mr_pd_bt_rcvr signal control the power to the analog portion of the 10 BaseT receiver. A

22   mr_pd_lp signal controls the power to the link pulse circuit (inside the energy detect block).

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1   A mr_pd_en_det signal for control the energy detect circuit. A mr_pd_fx signal for

2   controlling the fx circuit and a mr_pwr_dwn signal for controlling the test, reference bias,

3   and transmit blocks.

4   Referring to Fig. 3, a power management logic control table of the present invention

5   is illustrated. Here, the operation modes are listed in the column titles and the various

6   control signals are listed in the row titles. Note that a signal of "1" powers down the

7   corresponding circuit. It can be seen that during the power down mode, all of the control

8   signals power down their corresponding circuit. During the energy detect mode, only the

9   mr_pd_en_det signal is activated. During the auto-negotiation mode, only the mr_pd_fx

10 signal powers down its corresponding circuit. During 10 BaseT operation, the circuits

11 corresponding to the mr_pd_pll, mr_bt_rcvr and mr_pd_en_det signals are active. During

12 100 BaseTx operation, the circuits corresponding to the mr_pd_pll, mr_pd_equal, and

13 mr_pd_en_det are active. For the FX mode, the circuits corresponding to mr_pd_pdd and

14 mr_pd_fx are active. In conducting test loopback, the circuits corresponding to mr_pd_pll,

15 mr_pd_equal, and mr_pd_fx signals are active. For PC bypass 10 operation, the circuits

16 corresponding mr_pd_pll, mr_bt_rcvr, and mr_pd_en_det signals are active. For PCS

17 bypass 100 operation, the circuits corresponding to mr_pd_pll, mr_pd_equal, and

18 mr_pd_en_det signals are active.

19   While the present invention has been described with reference to certain preferred

20 embodiments, it is to be understood that the present invention is not to be limited to such

21 specific embodiments. Rather, it is the inventor's intention that the invention be understood

22 and construed in its broadest meaning as reflected by the following claims. Thus, these

1   claims are to be understood as incorporating and not only the preferred embodiment

2   described herein but all those other and further alterations and modifications as would be

3   apparent to those of ordinary skill in the art.

4

What we claim are:

CLAIMS

1   1.   A transceiver circuit, said circuit comprising:

2   a transmitter, said transmitter transmitting a normal link pulse during idle period;

3   a number of clock signals, each controlling a portion of said transceiver; and

4   said transceivers circuit utilizing said clock signals for minimizing power

5   consumption.

ABSTRACT

A transceiver circuit having 10 mb and 100 mb transmit and receive circuitries using the power saving methods of the present invention is disclosed. The power consumption of the transceiver circuit can be significantly reduced by providing each defined subcircuit with its own power supply and means of activation and deactivation. However, the method for activating and deactivating digital subcircuits and analog subcircuits are different and therefore different types of control signals and methods are provided. Furthermore, there are two general types of power-saving situations. The first type is near total circuit power-down and the second type is partial circuit power-down. The present invention in yet another embodiment discloses a method for minimizing energy usage during idle period.

Fig. 1a

Fig. 1b

Fig. 1c
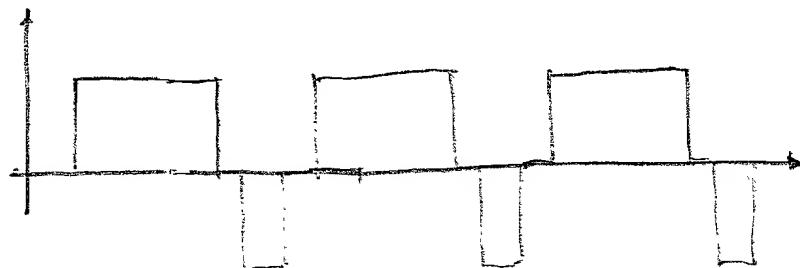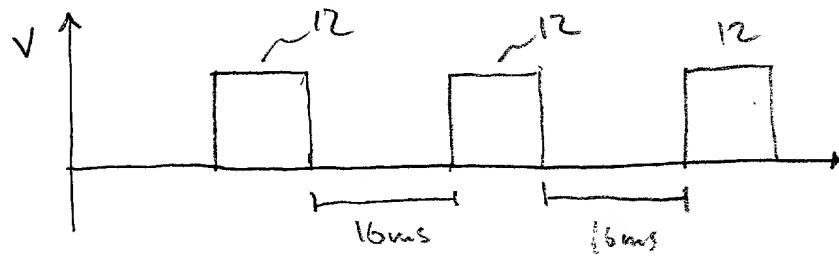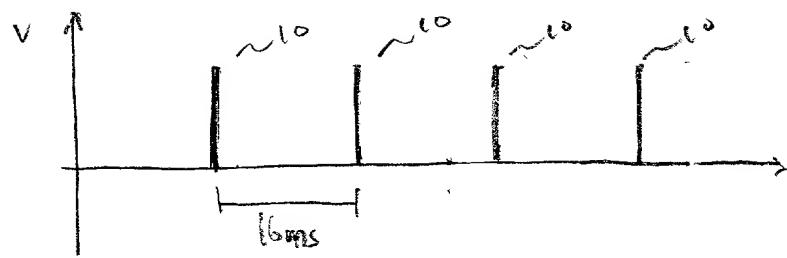
Clock Name	Power Down	Energy Detect	Auto-Neg	10 Base T	100 Base TX	Serial 10 BT	FX Mode	Test Loopback	PCS bypass 10	PCS bypass 100
bt_txc_20	OFF	OFF	OFF	20	OFF	20	OFF	OFF	20	OFF
bt_rxc_20	OFF	OFF	OFF	20	OFF	20	OFF	OFF	20	OFF
tx_txc	OFF	OFF	OFF	OFF	25	OFF	25	25	OFF	OFF
tx_rxc	OFF	OFF	OFF	OFF	25	OFF	25	25	OFF	25
mii_txc	OFF	25/2.5	25	2.5	25	10	25	25	20	25
mii_rxc	OFF	OFF	OFF	2.5(a)	25(a)	10(a)	25(a)	25(a)	OFF	25
cp_arb	OFF	ON	25	25	OFF	25	OFF	OFF	OFF	OFF

Fig. 2

Signal Name	Power Down	Energy Detect	Auto-Neg	10 Base T	100 Base TX	FX Mode	Test Loopback	PCS bypass 10	PCS bypass 100
mr_pd_pll	1	1	0	0	0	0	0	0	0
mr_pd_equal	1	1	0	1	0	1	0	1	0
mr_bt_rcvr	1	1	0	0	1	1	1	0	1
mr_pd_lp	1	1	0	1	1	1	1	1	1
mr_pd_en_det	1	0	0	LINK	LINK	1	1	LINK(a)	LINK(b)
mr_pd_fx	1	1	1	1	1	0	0	1	1

Fig. 3

DECLARATION, POWER OF ATTORNEY AND PETITION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **"Methods and Circuits for Power Management in a Transceiver"**, the specification of which

(check one)   ☒ is attached hereto

                ☐ was filed on_____ as Application Serial No._____

                and was amended on _____ *(if applicable).*

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) or U.S. provisional application(s) for patent or inventor's certificate listed below and have also identified below any foreign application or U.S. provisional application(s) for patent or inventor's certificate having a filing date before that of the application of which priority is claimed.

Prior Foreign/U.S. Provisional Application(s)

Priority Claimed

U.S. Provisional Application entitled "Reset and Power Management" filed on October 8, 1998   **X**   ___

(Number)	(Country)	(Day, month, year filed)	Yes	No
(Number)	(Country)	(Day, month, year filed)	Yes	No
(Number)	(Country)	(Day, month, year filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	Filing Date	(Status: Patented, pending, abandoned)
(Application Serial No.)	Filing Date	(Status: Patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

And I hereby appoint W. POMS, Reg. 18,782; G.P. SMITH, Reg. 20,142; G.E. LANDE, Reg. 22,222; A.C. ROSE, Reg. 17,047; L.J. BOVASSO, Reg. 24,075; D.J. OLDENKAMP, Reg. 29,421; C. DARROW, Reg. 30,166; M.E. HARRIS, Reg. 26,690; K.A. MACLEAN, Reg. 31,118; C. ROSENBERG, Reg. 31,464; M.E. BROWN, Reg. 28,590; E.F. O'CONNOR, Reg. 25,903; R.F. CARR, Reg. 17,110; A. ROTHENBERG, Reg. 17,843; R.L. GAUSEWITZ, Reg. 16,960; M.A. KONDZELLA, Reg. 18,013; A.P. BLOCK, Reg. 35,450; S.R. HANSEN, Reg. 38,486; D.N. LARSON, Reg. 29,401; J.W. INSKEEP, Reg. 33,910; G.F. COTTERELL, Reg. 37,802; H.D. JASTRAM, Reg. 19,777; C.J. LERVICK, Reg. 35,244; C.A.S. HAMRICK, Reg. 22,586; R.O. GUILLOT, Reg. 28,852; J.D. VOELZKE, Reg. 37,957; G.L. FOUNTAIN, Reg. 36,374;

J. BOYCE, Reg. 40,920; C. CHOU, Reg. 41,672; A.B. DIEPENBROCK, Reg. 39960; M.K. BOSWORTH, Reg. 28,186, OPPENHEIMER WOLFF & DONNELLY LLP, 3373 Hillview Avenue, Suite 200, Palo Alto, California 94304, (650) 320-4000, as my attorneys with full power of substitution and revocation, to prosecute said application and to transact in connection therewith all business in the Patent and Trademark Office and before competent International Authorities.

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Wherefore I pray that Letters Patent be granted to me for the invention or discovery described and claimed in the foregoing specification and claims, and I hereby subscribe my name to the foregoing specification and claims, declaration, power of attorney, and this petition.

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